

CLAIMS

What is claimed is:

- 1 1. A computer system comprising a memory controller that includes a slot-based controller, wherein the slot-based controller is adaptable to launch a packet that straddles a first fixed packet slot and a second fixed packet slot.
- 1 2. The computer system of claim 1 wherein the packet launch position is advanced one half of a slot position relative second fixed packet slot.
- 1 3. The computer system of claim 1 wherein the packet is tagged with an attribute that indicates that the packet is straddling the first fixed packet slot and the second fixed packet slot.
- 1 4. The computer system of claim 3 wherein the attribute is a Rambus clock offset.
- 1 5. The computer system of claim 1 wherein the packet is a Rambus control packet.
- 1 6. The computer system of claim 1 wherein the memory controller further comprises a Rambus Asic Cell (RAC), wherein the RAC interfaces with a high frequency expansion channel.
- 1 7. The computer system of claim 6 wherein the slot-based controller comprises:
 - 2 a scheduler;
 - 3 a rules checker coupled to the scheduler;
 - 4 a future packet queue coupled to the scheduler and the rules checker; and
 - 5 a past packet queue coupled to the future packet queue, the scheduler and the rules checker.

1 8. The computer system of claim 6 wherein the rules checker uses entries in the past
2 packet queue to validate future slot choices for the scheduler.

1 9. The computer system of claim 7 wherein the past packet queue and the future
2 packet queue are unidirectional shift registers.

1 10. The computer system of claim 7 wherein the slot-based controller further
2 comprises packet driving logic coupled to the RAC and the scheduler.

1 11. The computer system of claim 6 further comprising:
2 an expansion channel coupled to the RAC within the memory controller; and
3 a repeater coupled to the expansion channel.

1 12. The computer system of claim 11 further comprising:
2 a stick channel coupled to the repeater; and
3 a plurality of memory devices coupled to the stick channel.

1 13. The computer system of claim 12 wherein the memory devices are Rambus
2 Dynamic Random Access Memories (RDRAMs).

1 14. The computer system of claim 11 further comprising a plurality of memory
2 devices coupled to the expansion channel.

1 15. A memory controller comprising a slot-based controller adaptable to launch a
2 packet that straddles a first fixed packet slot and a second fixed packet slot.

1 16. The memory controller of claim 15 wherein the packet launch position is
2 advanced one half of a slot position relative second fixed packet slot.

1 17. The memory controller of claim 15 wherein the packet is tagged with an attribute
2 that indicates that the packet is straddling the first fixed packet slot and the second fixed
3 packet slot.

1 18. The memory controller of claim 17 wherein the attribute is a Rambus clock offset.

1 19. The memory controller of claim 15 wherein the packet is a Rambus control
2 packet.

1 20. The memory controller of claim 15 wherein the memory controller further
2 comprises a Rambus Asic Cell (RAC), wherein the RAC interfaces with a high frequency
3 expansion channel.

1 21. The memory controller of claim 20 wherein the slot-based controller comprises:
2 a scheduler;
3 a rules checker coupled to the scheduler;
4 a future packet queue coupled to the scheduler and the rules checker; and
5 a past packet queue coupled to the future packet queue, the scheduler and the
6 rules checker.

1 22. The memory controller of claim 21 wherein the rules checker uses entries in the
2 past packet queue to validate future slot choices for the scheduler.

1 23. The memory controller of claim 21 wherein the past packet queue and the future
2 packet queue are unidirectional shift registers.

1 24. The memory controller of claim 21 wherein the slot-based controller further
2 comprises packet driving logic coupled to the RAC and the scheduler.

1 25. A slot-based controller comprising:
2 a scheduler;
3 a rules checker coupled to the scheduler;
4 a future packet queue coupled to the scheduler and the rules checker; and
5 a past packet queue coupled to the future packet queue, the scheduler and the
6 rules checker;
7 wherein the slot-based controller is adaptable to launch a packet in
8 advance of a predetermined packet slot.

1 26. The slot-based controller of claim 25 wherein the advance packet launch is
2 accomplished by straddling the packet on a first fixed packet slot and a second fixed
3 packet slot, wherein the first packet slot is designated for a previously scheduled packet.

1 27. The memory controller of claim 25 wherein the past packet queue and the future
2 packet queue are unidirectional shift registers.

1 28. The memory controller of claim 25 wherein the slot-based controller further
2 comprises packet driving logic coupled to the RAC and the scheduler.